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MS-7418 (MS-6496)

Version 0A

CPU:

Intel Dimondville

System Chipset:

Intel 945GC (North Bridge)

Intel ICH7(South Bridge)

On Board Chipset:

BIOS -- FWH FLASH 4Mb

HD AUDIO CODEC(ALC888)

LAN -- Realtek RTL8111C

Clock Generator - ICS954119

Main Memory:

DDR II SO-DIMM x 1 (Max 2GB)

CF Card Connector for flash Memory

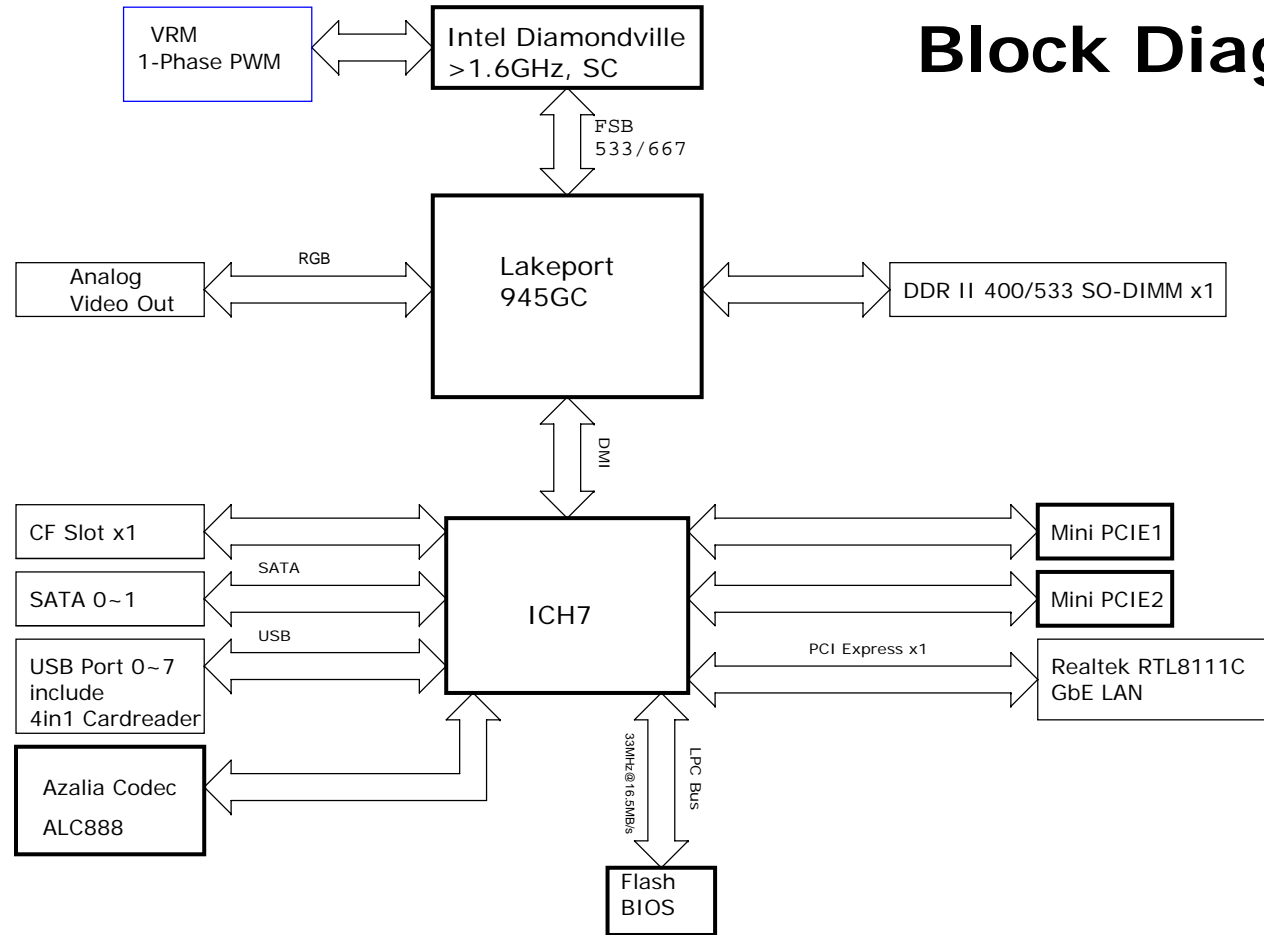
Expansion Slots:

Internal Mini PCI x 1

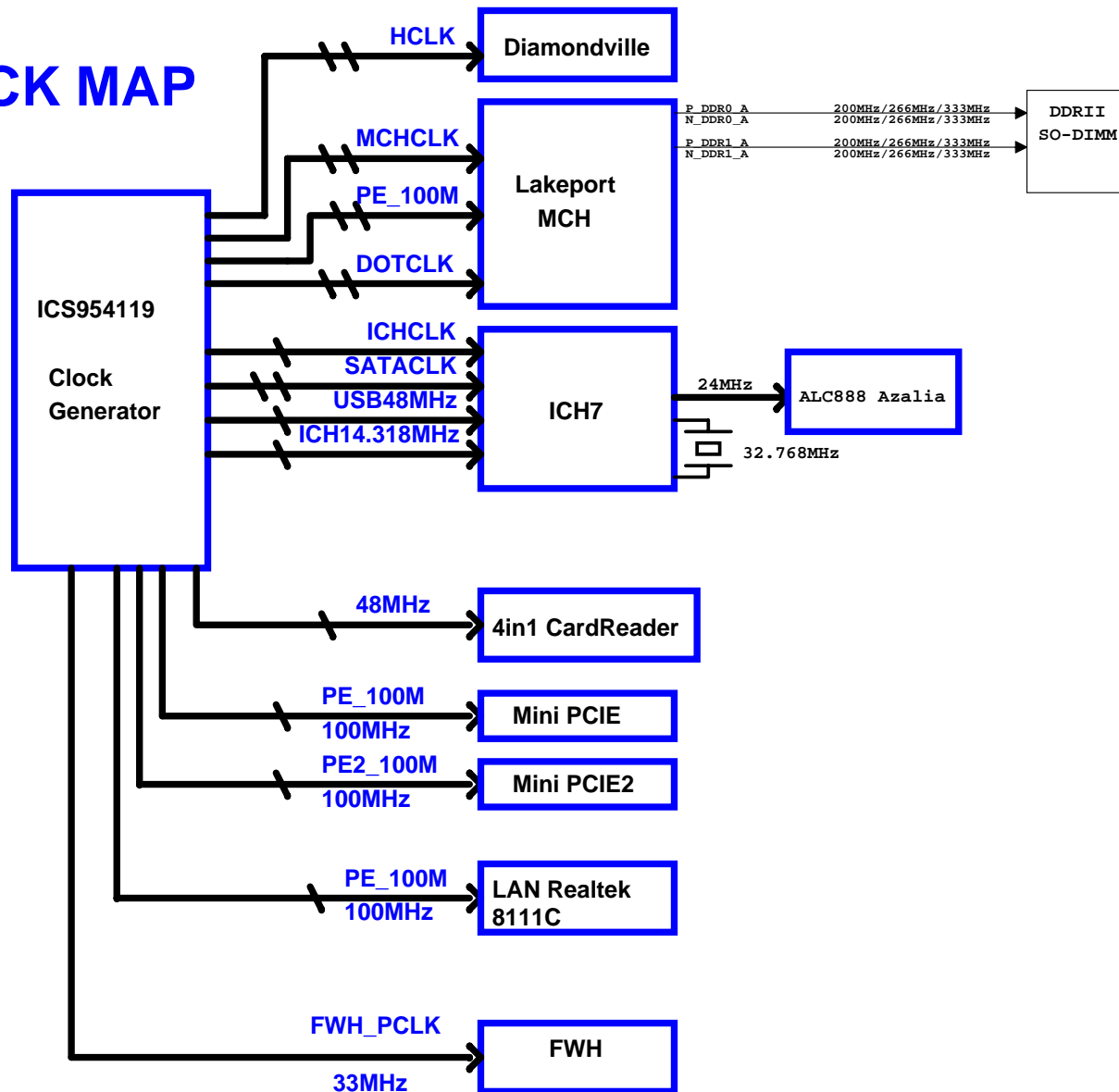
Intersil PWM:

Controller: ISL6326CR

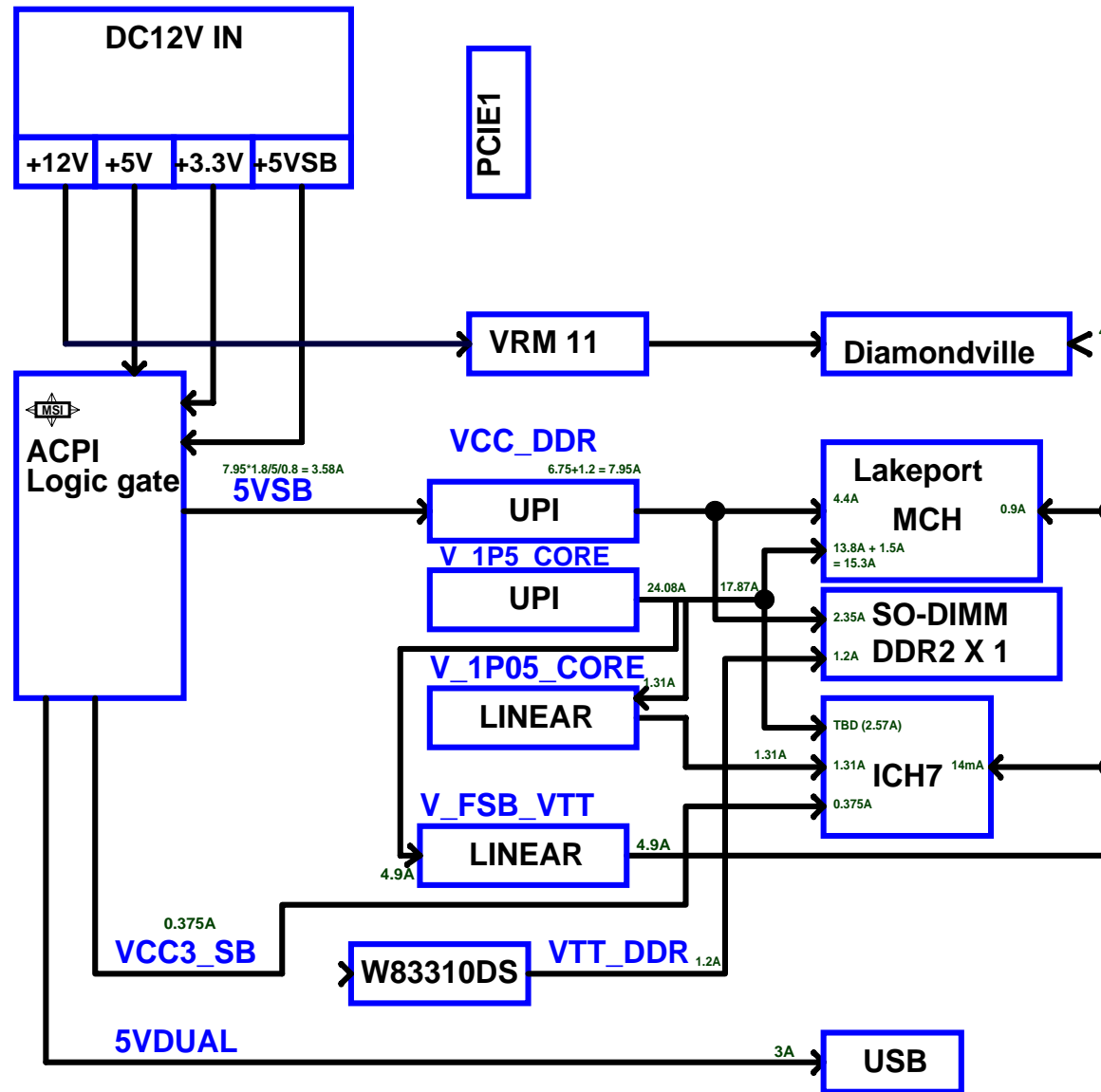
Block Diagram



CLOCK MAP



POWER MAP



ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name or status
GPIO[0]	SIO_SMI#	AB18	I/O	Vcc3p3	N	Y	5	Input	pull high VCC3
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	ATADET0	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	GPI7	AC18	I/O	Vcc3p3	N	Y	3.3	Input	pull high VCC3
GPIO[8]	SIO_PME#	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME# pull high VCC3_SB
GPIO[9]	WLAN_PWRON	E20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[14]	ADT7467_ALERT	R4	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	NC
GPIO[25]	S1_3_LED	D20	I/O	VccSus3p3	Y	N	3.3	1	pull high VCC3_SB
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#2	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#5
GPIO[30]	OC#2	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#6
GPIO[31]	OC#2	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#7
GPIO[32]	CLEAR_CMOS#	AG18	I/O	Vcc3p3	N	N	3.3	1	CLEAR_CMOS#, ONLY pull high VCC3
GPIO[33]	BIOS_WP#	AC19	I/O	Vcc3p3	N	N	3.3	1	BIOS_WP#
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	GNT4#
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD
GPI[15..0] can configured to cause a SMI# or SCI.									

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39;36;23;21;19;7;0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31;29;15;8]: default as inputs and should be pulled up to VccSus3_3 if unused.

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these				
GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-down
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

SIGNAL	DEVICE
MiniPCleRST#	MINI PCIE SLOT
TPMRST#	TPM
LANRST#	LAN 8111C
PCIRST_ICH7#	BUFFER IC
CF_RST#	CF_CARD
H_CPURST#	CPU
FWHRST#	FWH
MCHRST#	MCH

SMBCLK, SMBDATA, DDR2, PCIEX1, CLKGEN, ICH7, ADT7464

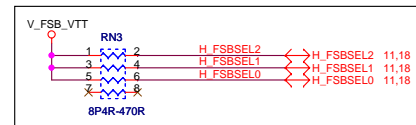
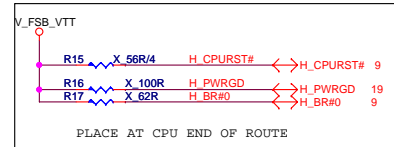
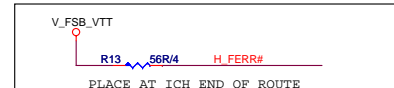
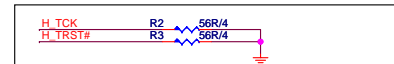
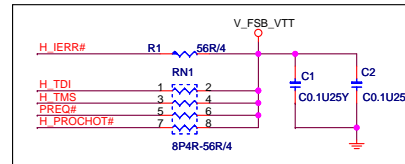
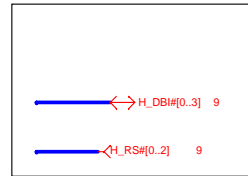
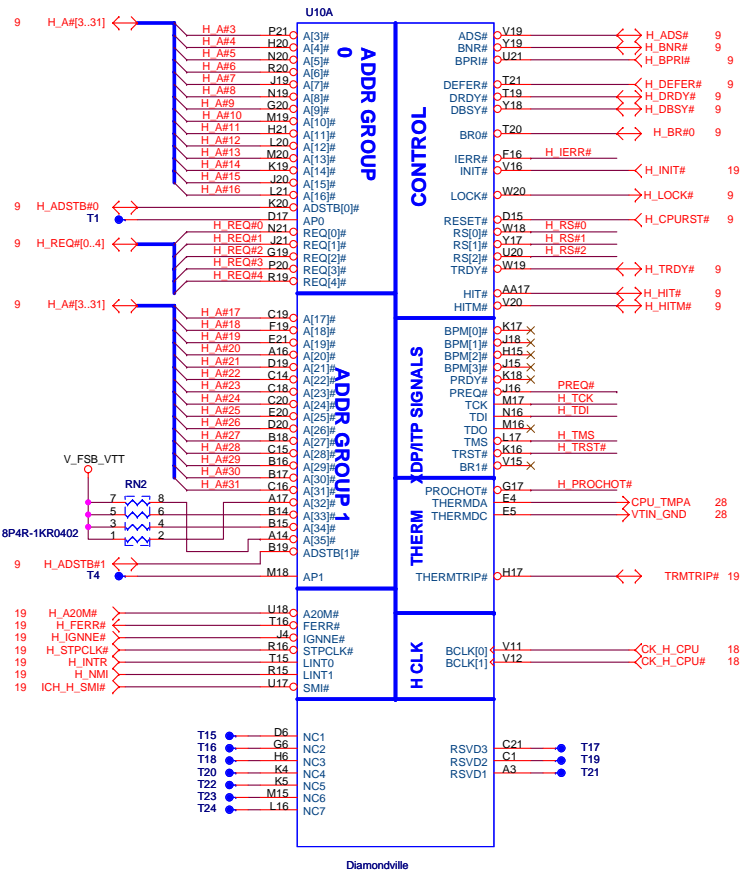
DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2

JUMPER SETTING

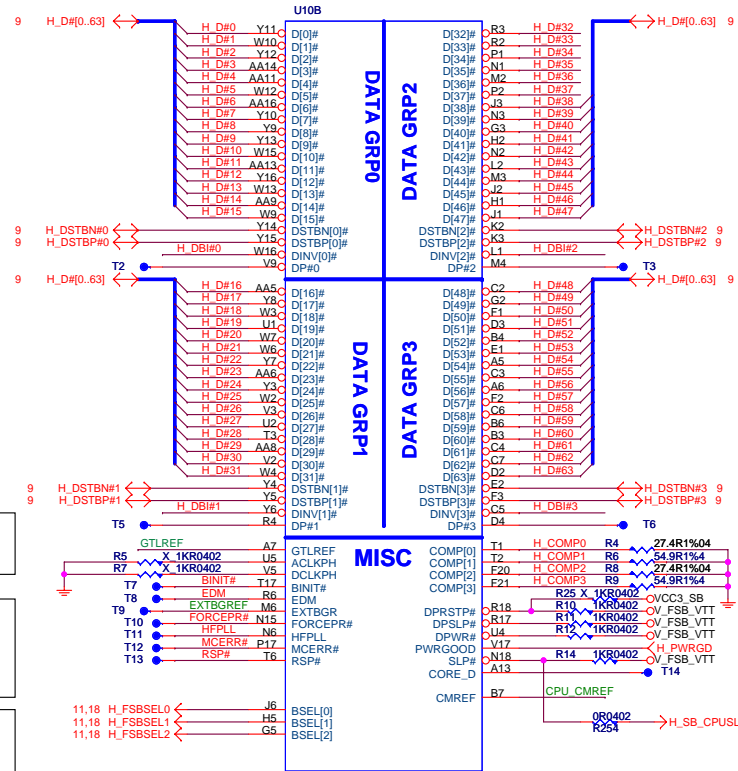
JBAT1	(1-2)NORMAL	(2-3)CLEAR
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CPU SIGNAL BLOCK

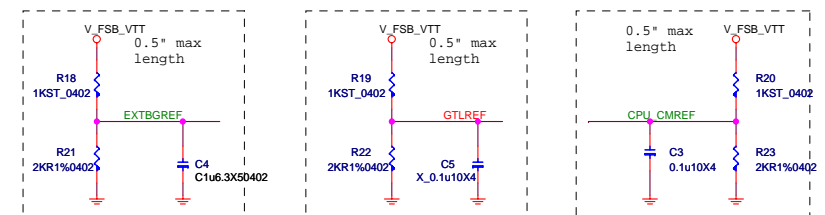


BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	1	133 MHZ (533)

For Diamondville processor
, the BSEL is fixed to operate
at 133-MHz BCLK frequency.



0.5" max length
25 MIL AWAY FROM HIGH
SPEED SIGNAL



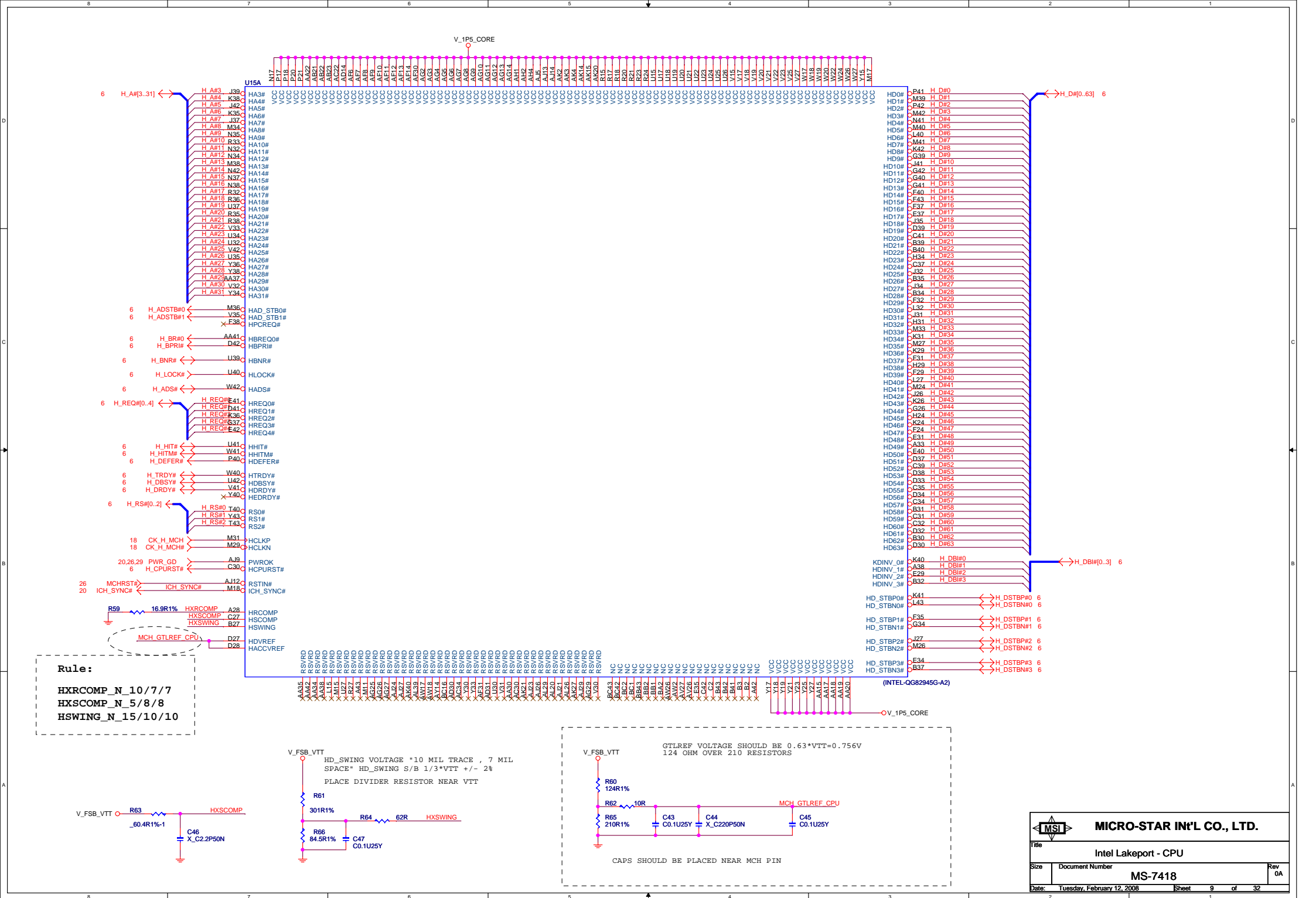
MICRO-STAR INT'L CO., LTD.

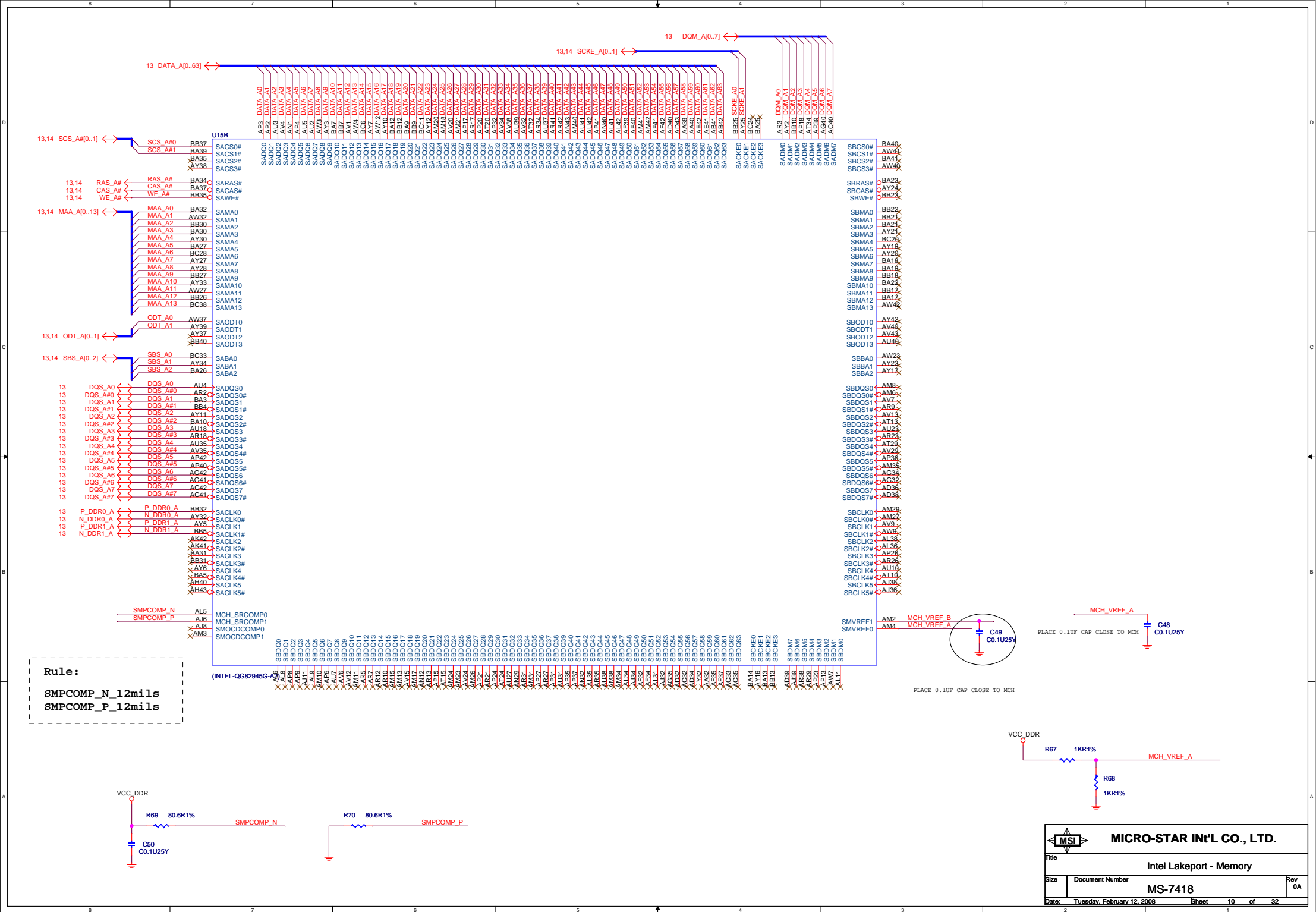
Title	Intel LGA775 - Signals
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Size	Document Number	Rev
	MS-7418	0A

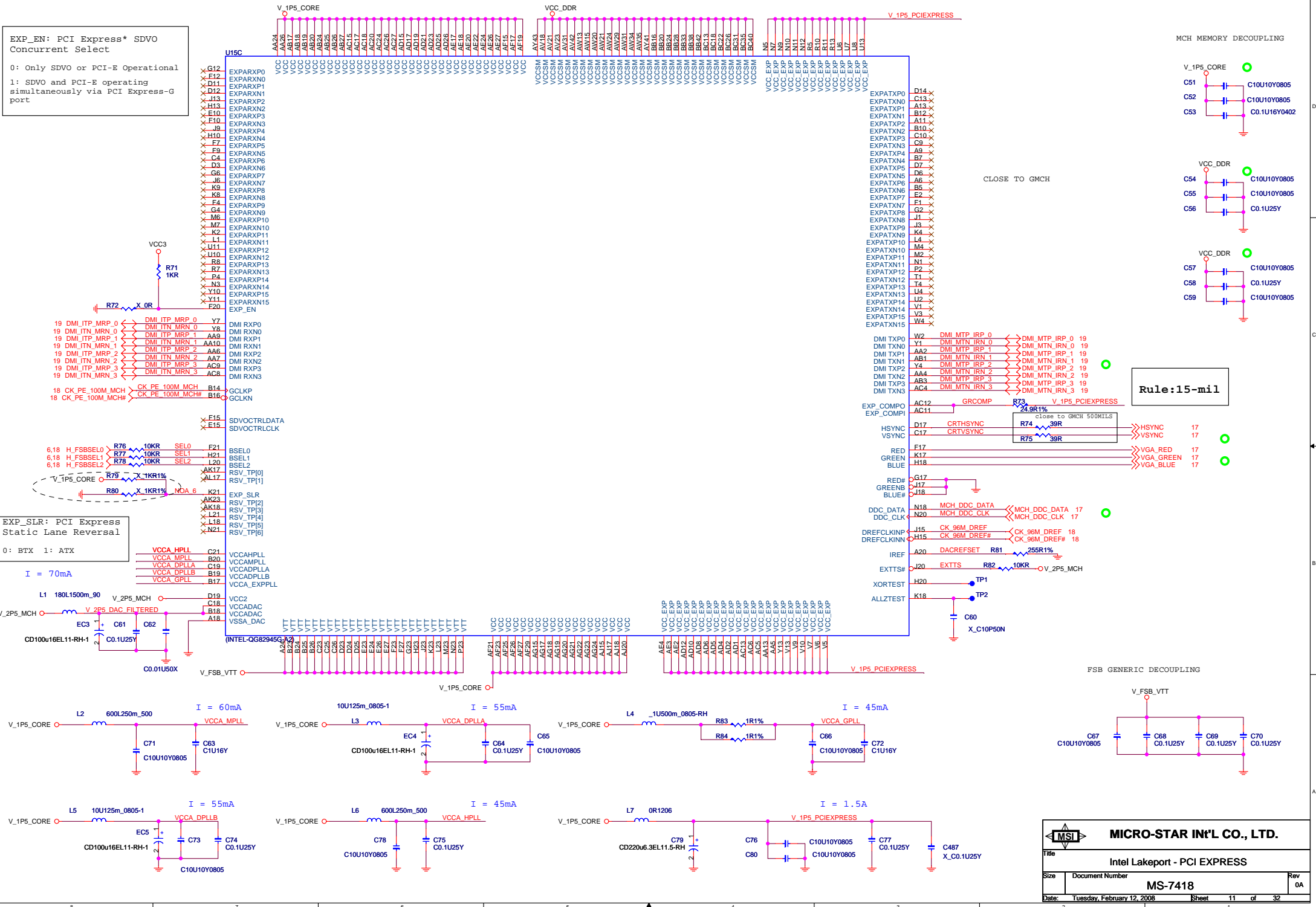
Date: Tuesday, February 12, 2008		Sheet 6 of 32	
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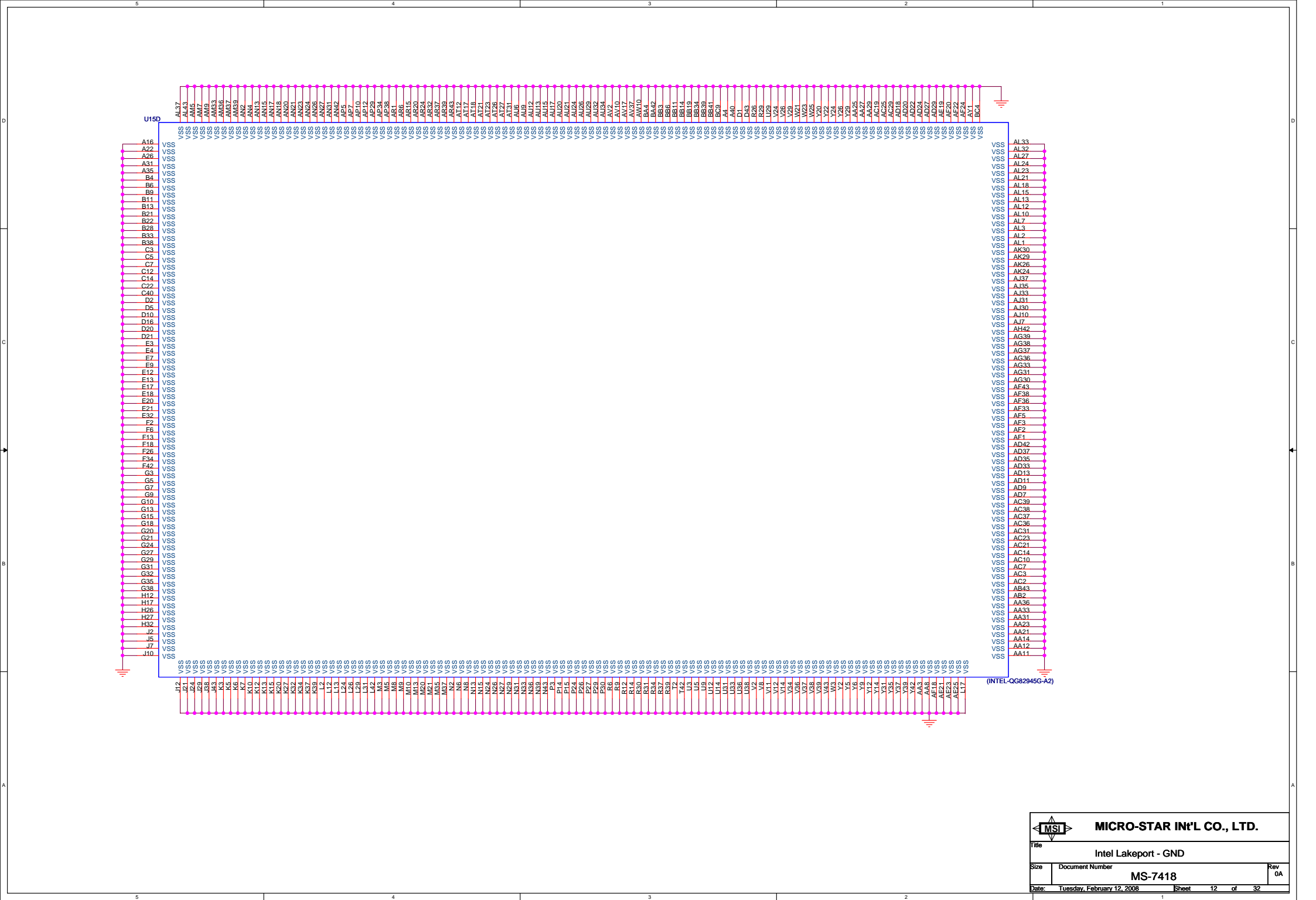
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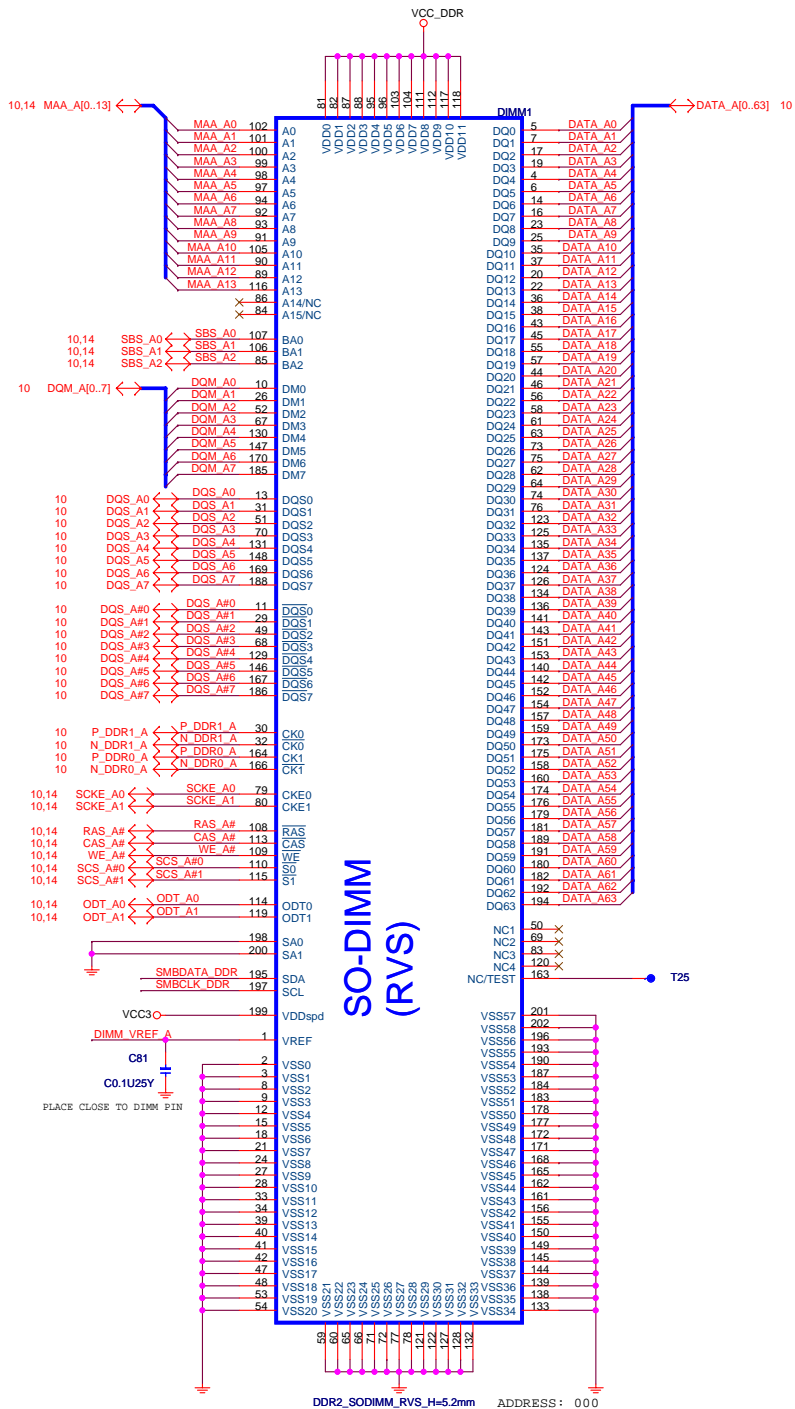


```
0: Only SDVO or PCI-E Operational
1: SDVO and PCI-E operating
simultaneously via PCI Express-G
port
```

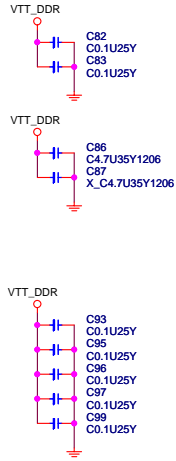




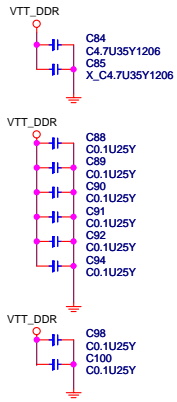
DDR2 SO-DIMM



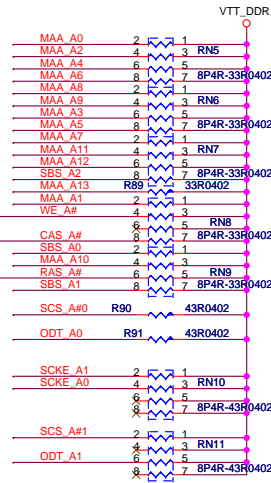
CHANNEL A V_SM_VTT
DECOULPING CAPS



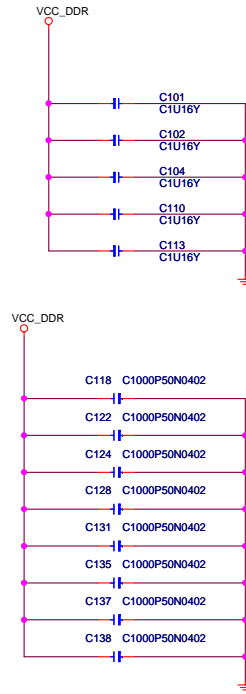
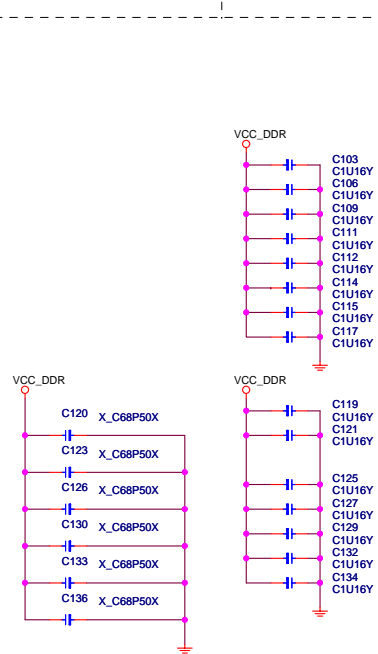
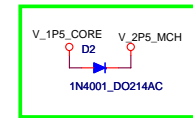
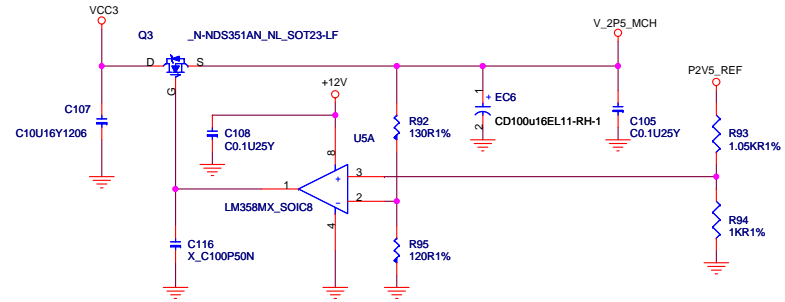
CHANNEL B V_SM_VTT
DECOULPING CAPS

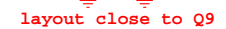
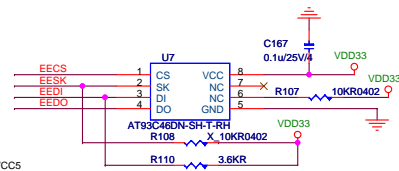
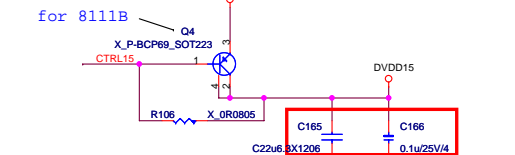
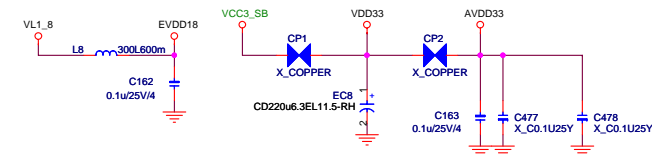
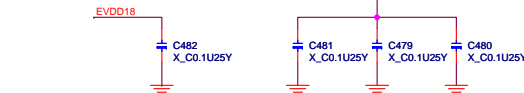
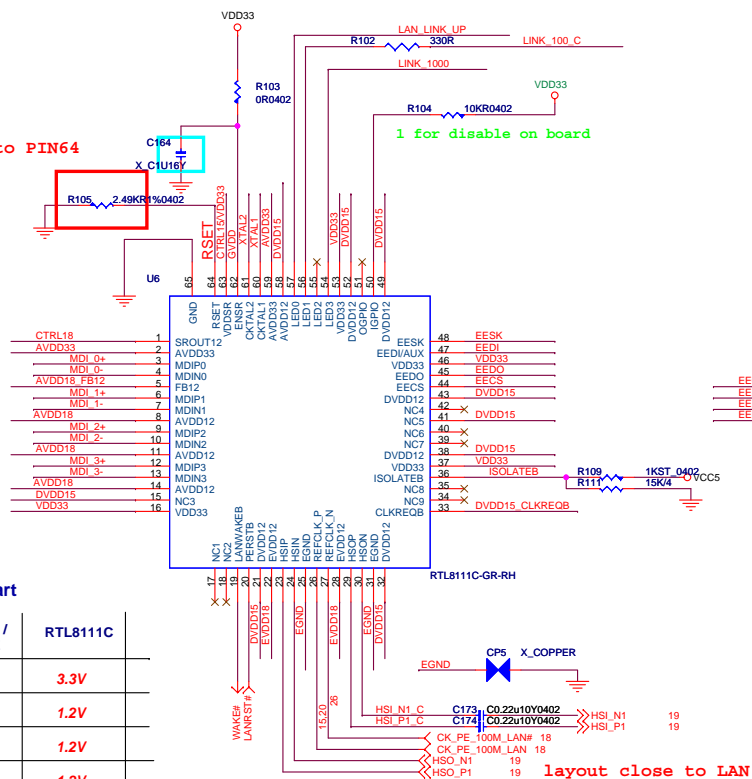


SCS_A#0 change 43 ohm



Grantsdale GMCH Power Sequencing
Requirement Between 1.5V Core and 2.5V DAC

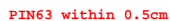
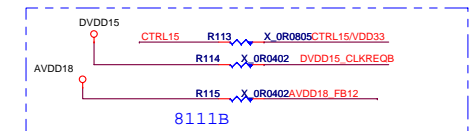
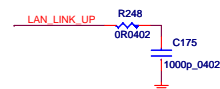
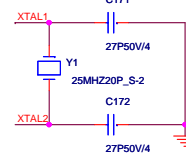












Power domain chart

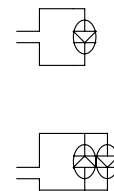
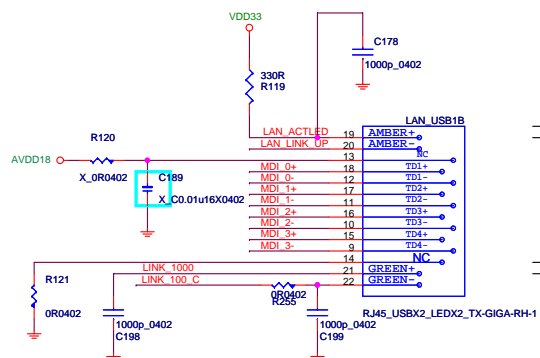
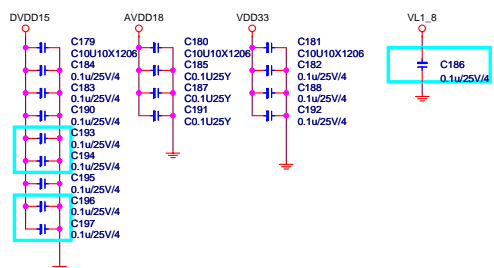
	RTL8111B / RTL8101E	RTL8111C	
AVDD33	3.3V	3.3V	
AVDD18	1.8V	1.2V	
EVDD18	1.8V	1.2V	
DVDD15	1.5V	1.2V	

	Q9	Q10
RTL8111B	<i>Need</i>	<i>Need</i>
RTL8111C	<i>N/A</i>	<i>N/A</i>



Power consumption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

Giga-Lan		10/100-Lan	
N58-22F0181-s42		N58-22F0061-s42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
	Yellow		Yellow
20		20	
21		21	
	Orange		
22		22	
	Green		Green



Video Connector

Power 20 mils

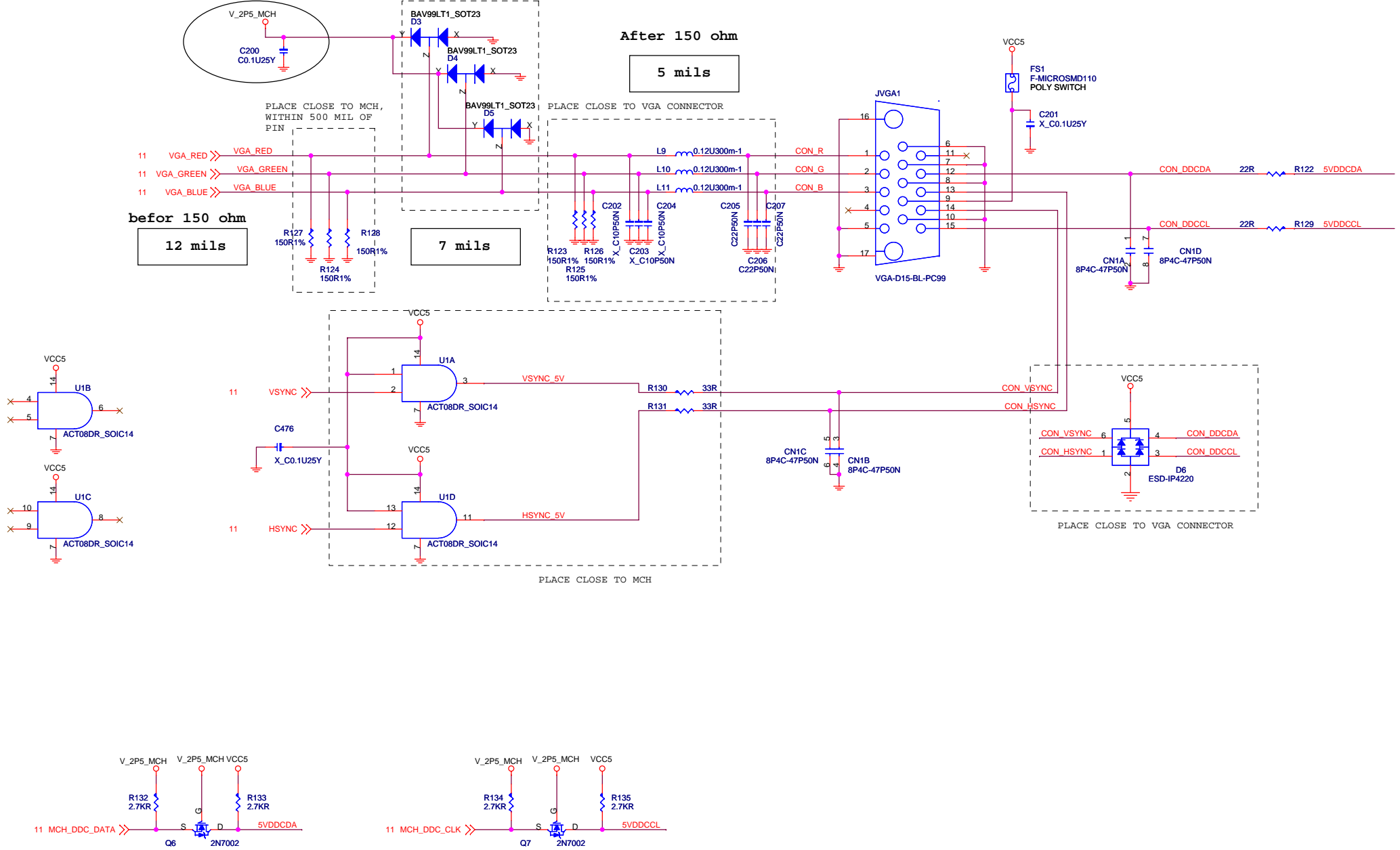
After 150 ohm

5 mils

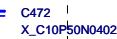
before 150 ohm

12 mils

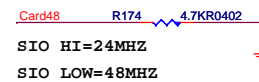
7 mils



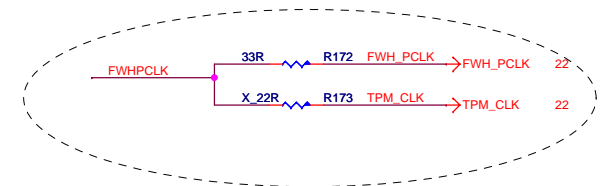
Trace length less than 0.5inches



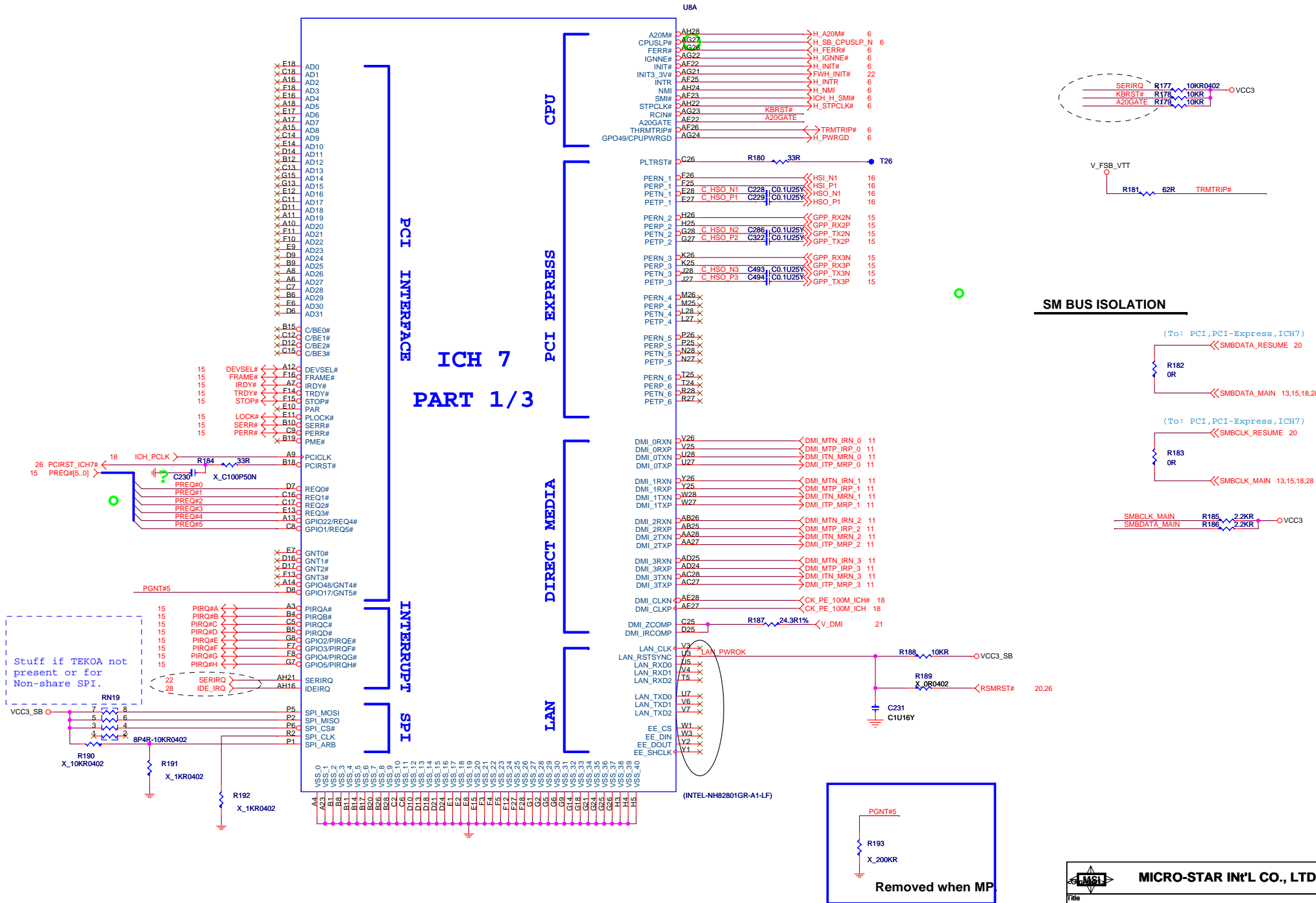
BSEL[0..2] Level Shift

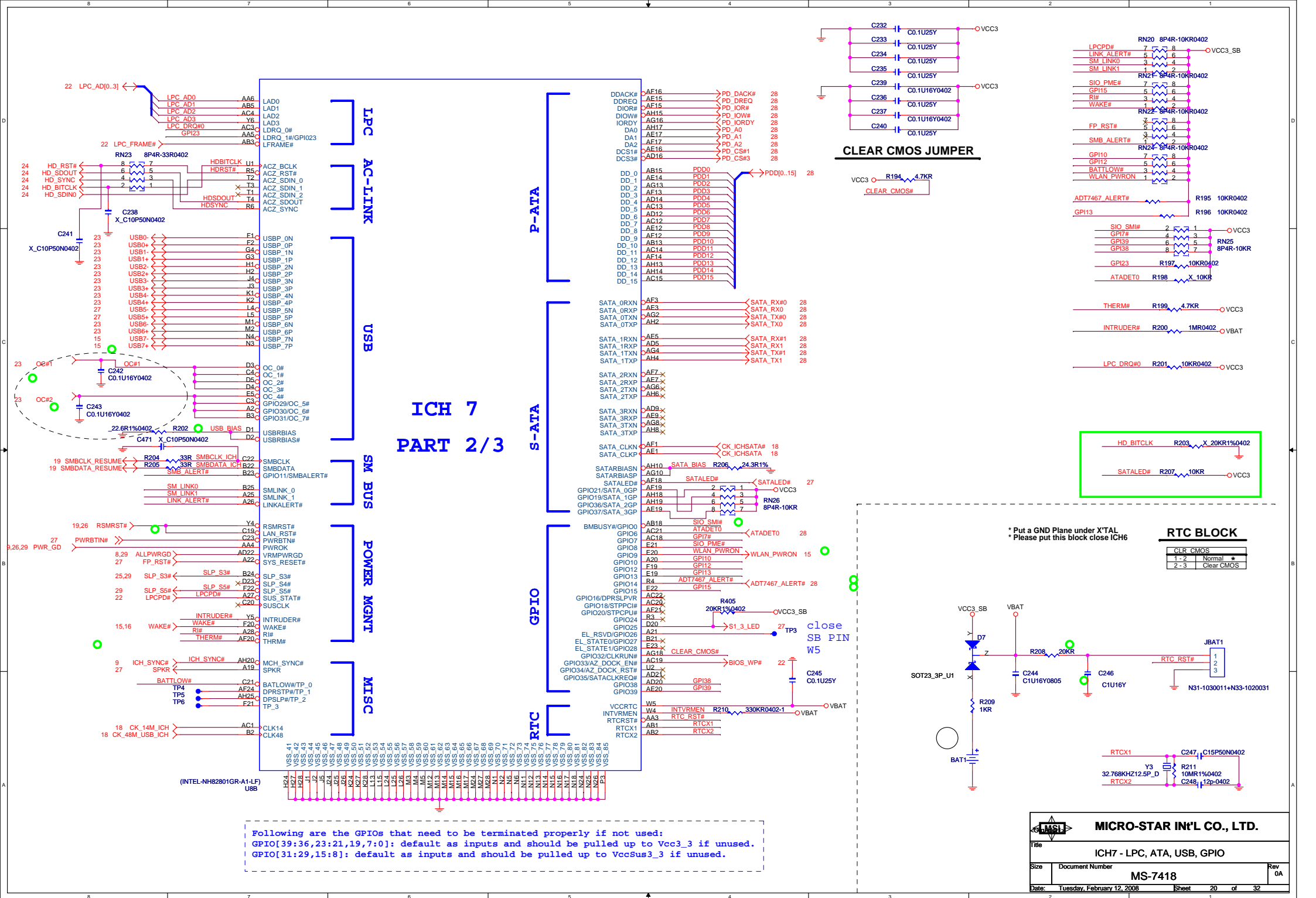


Clock Generator VTT Power Down Block

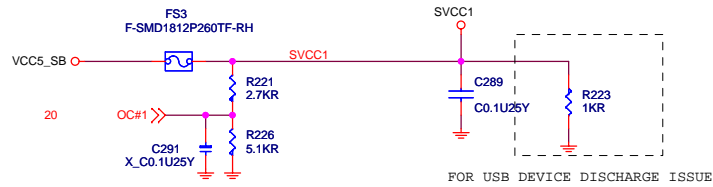


ICH 7 PART 1/3

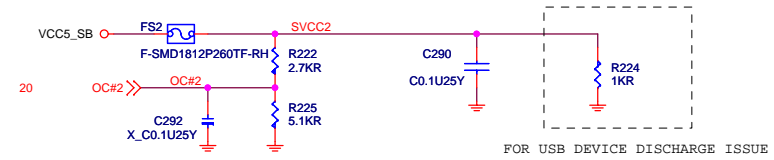




POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)

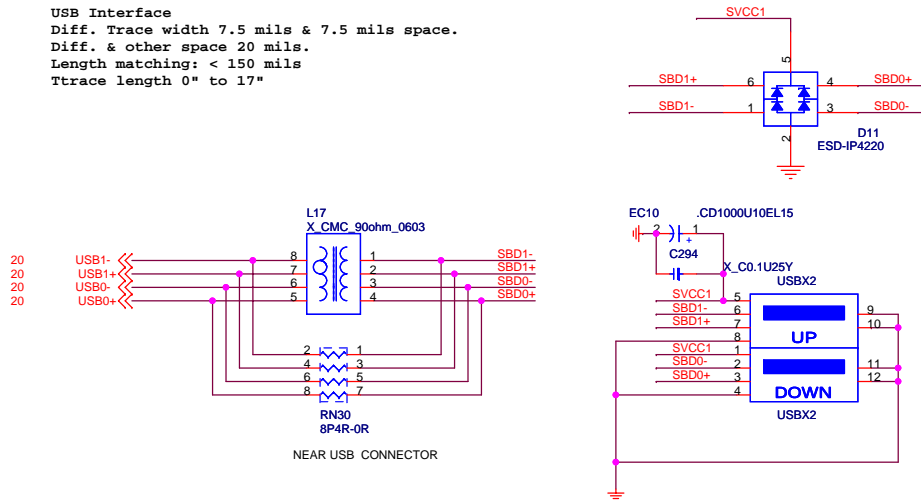


POWER CIRCUIT FOR USB PORT 4,6,7 (FRONT)



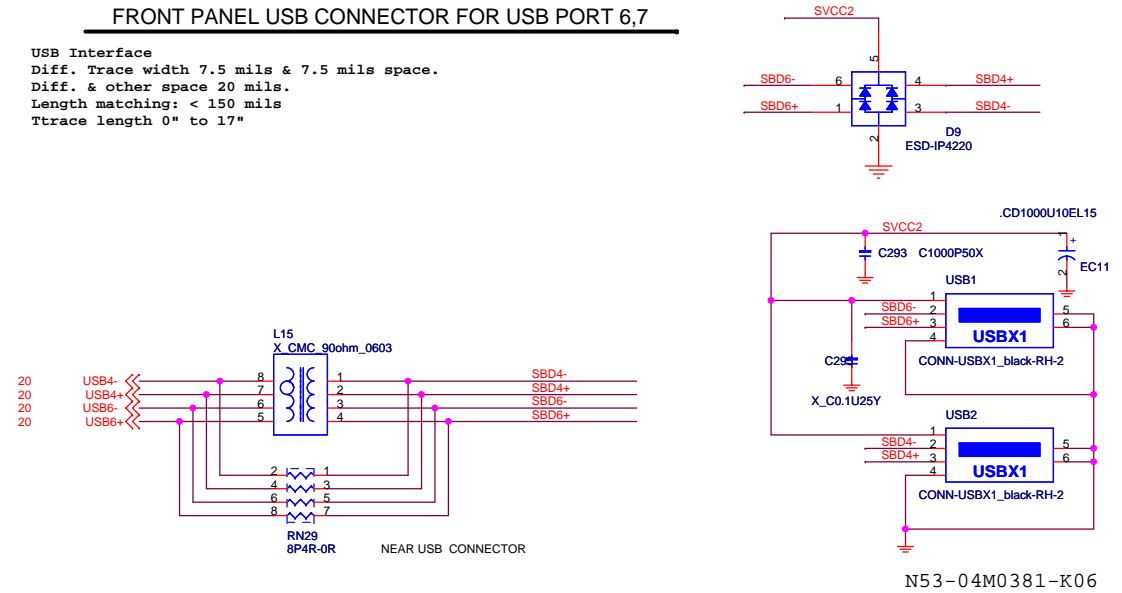
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"



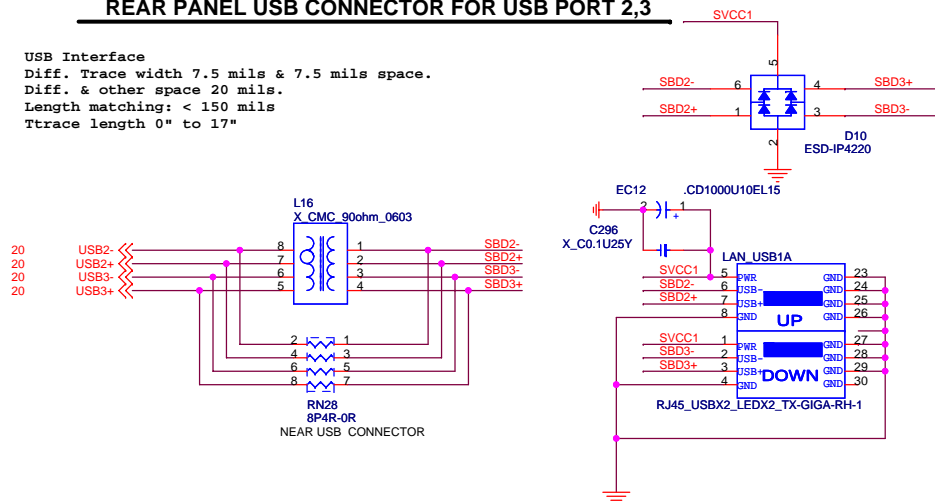
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"



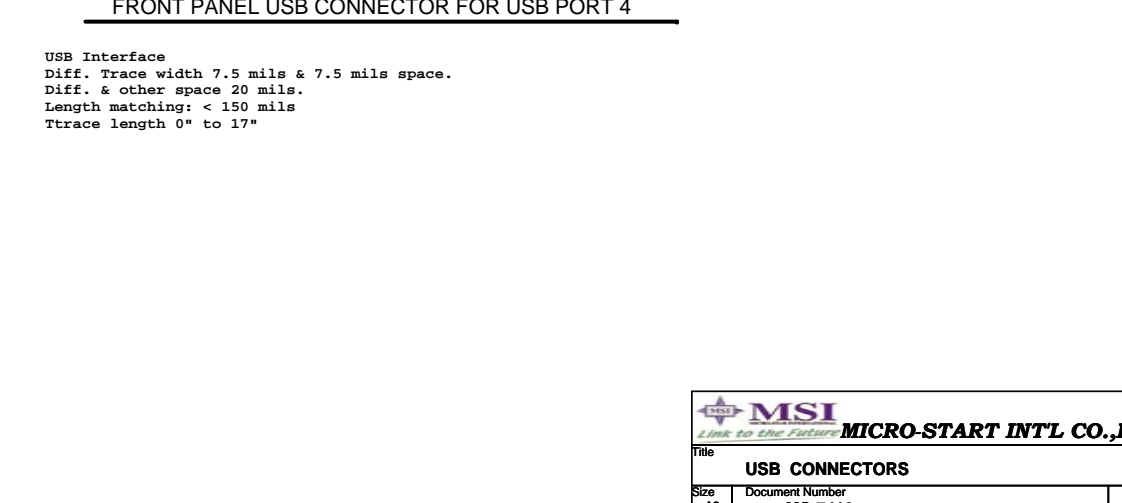
REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

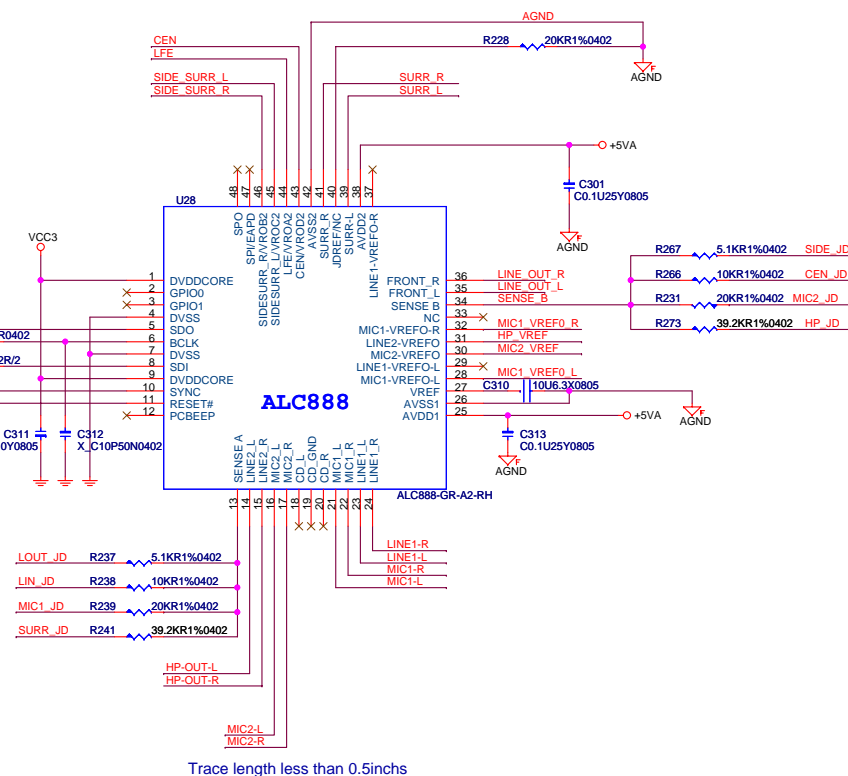


FRONT PANEL USB CONNECTOR FOR USB PORT 4

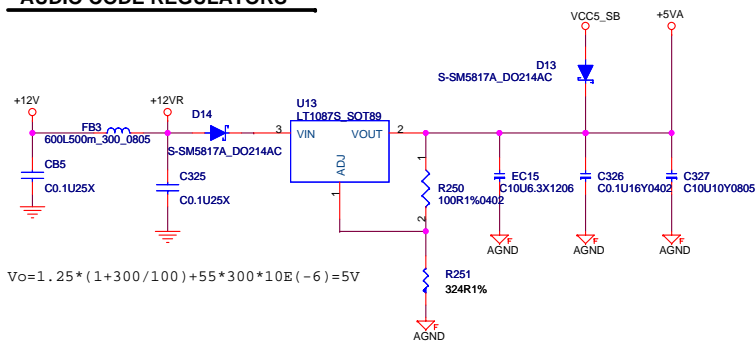
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"



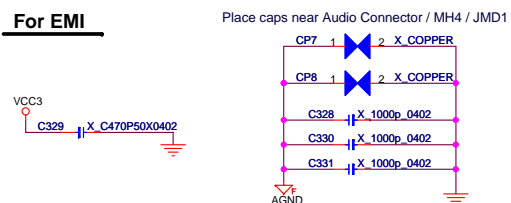
ALC888



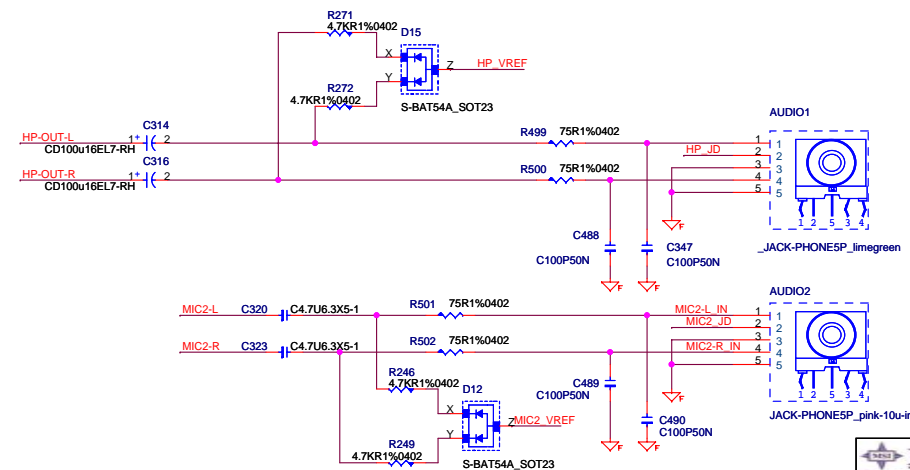
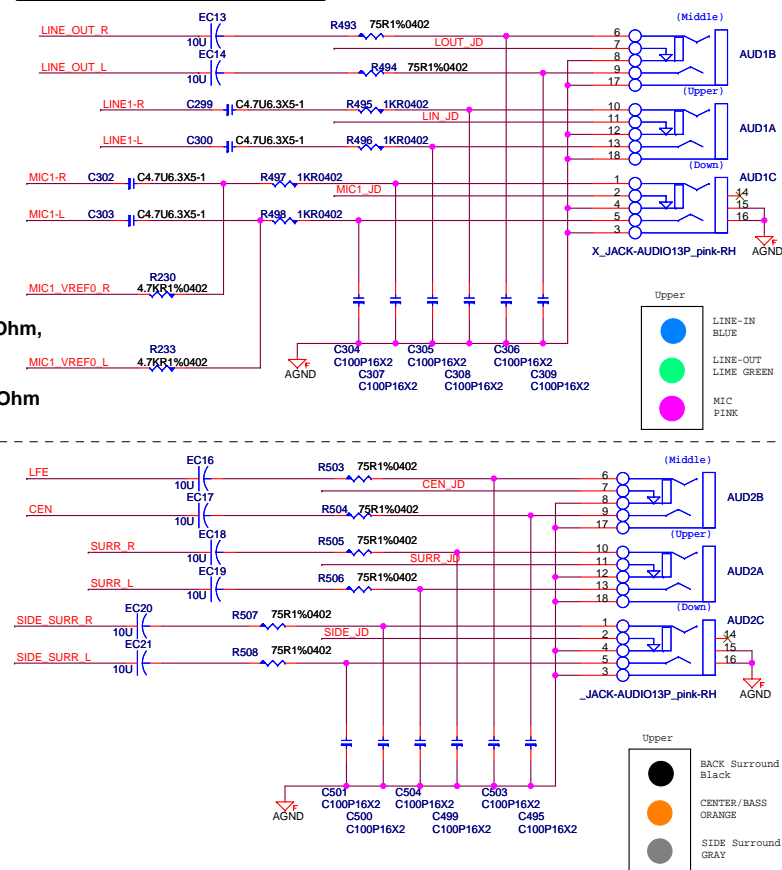
AUDIO CODE REGULATORS

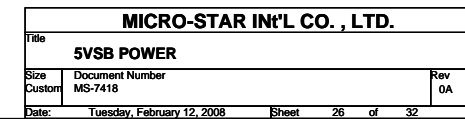
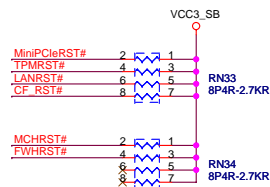


For EMI



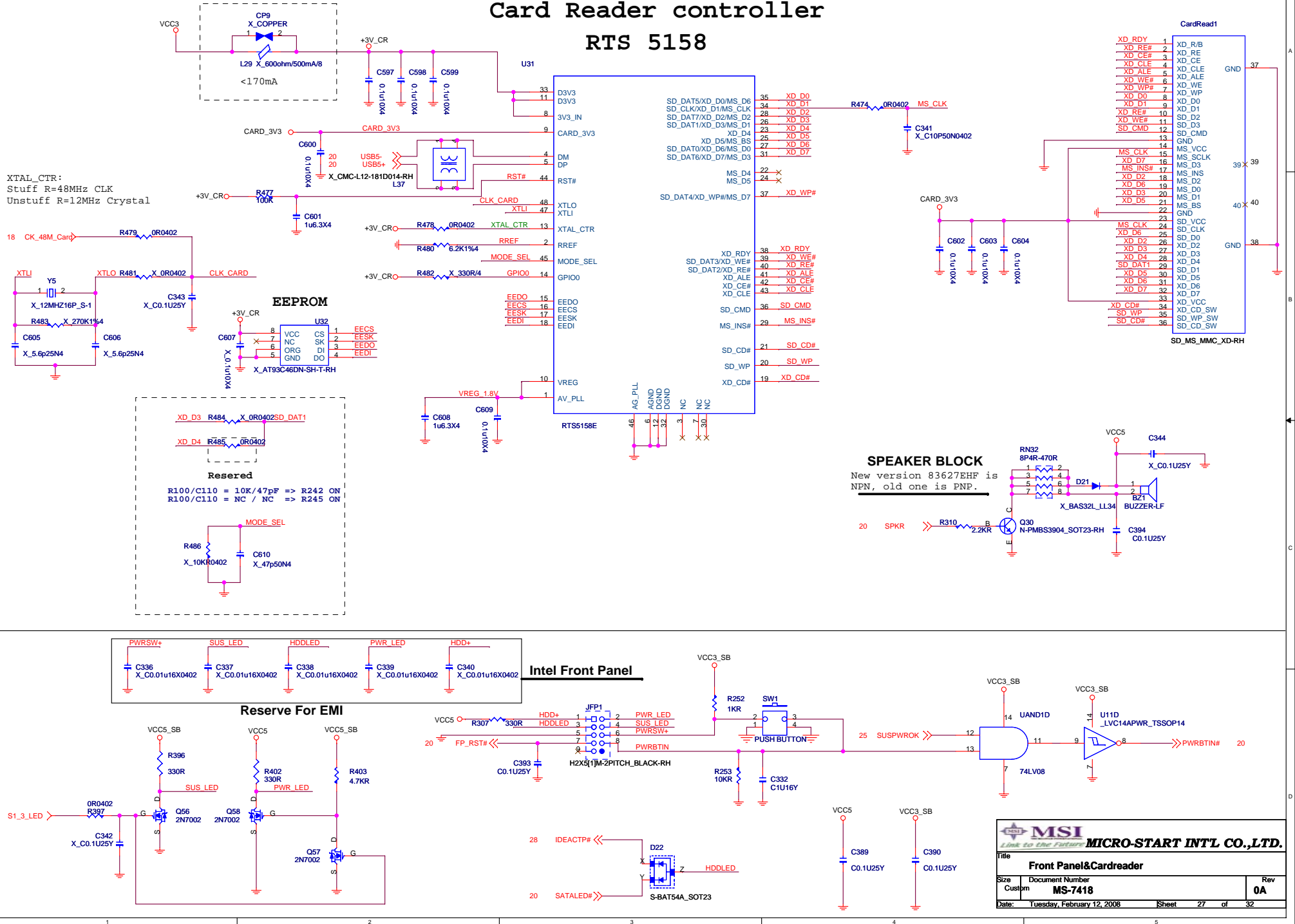
PHONE JACKER (HDA JACK)



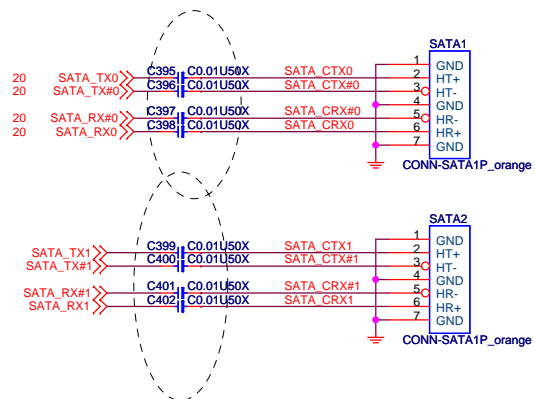


Flash Card Socket

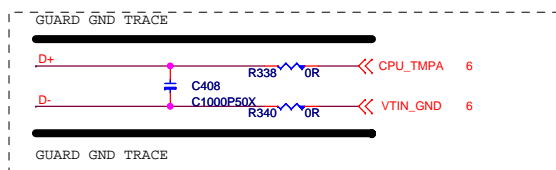
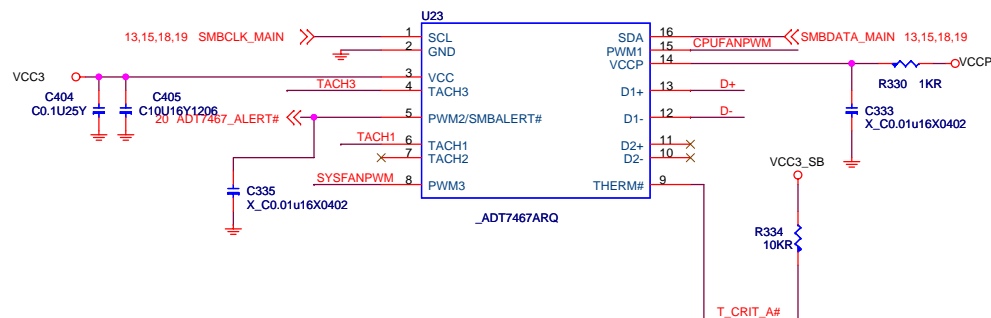
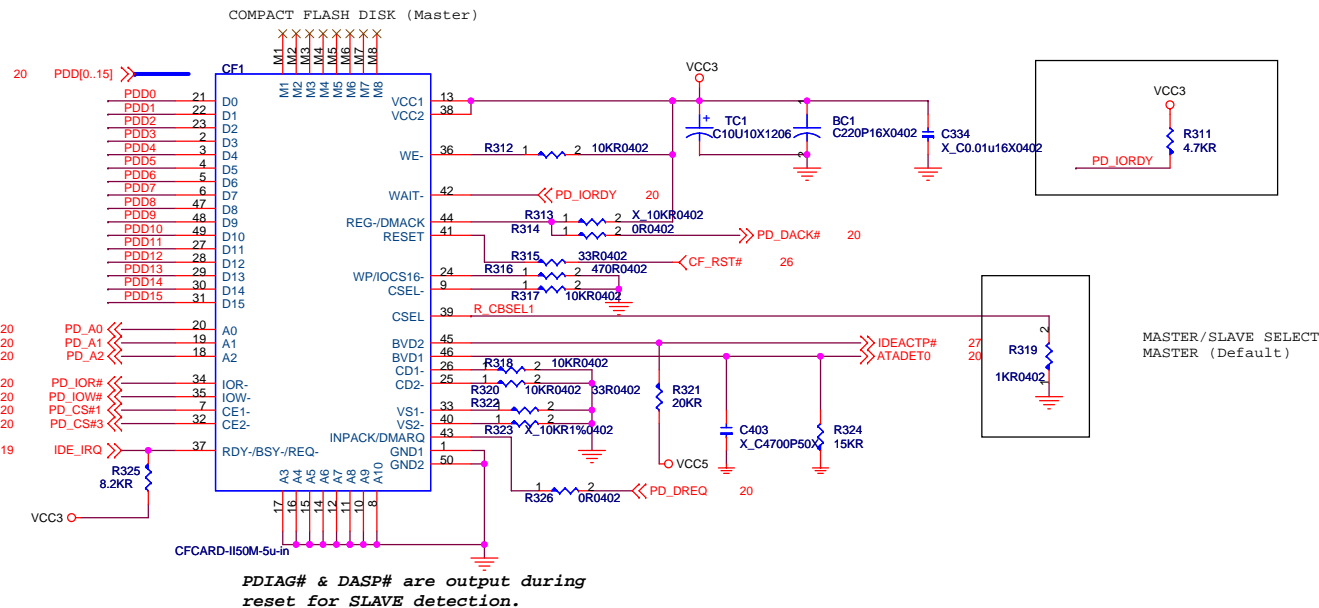
Card Reader controller RTS 5158



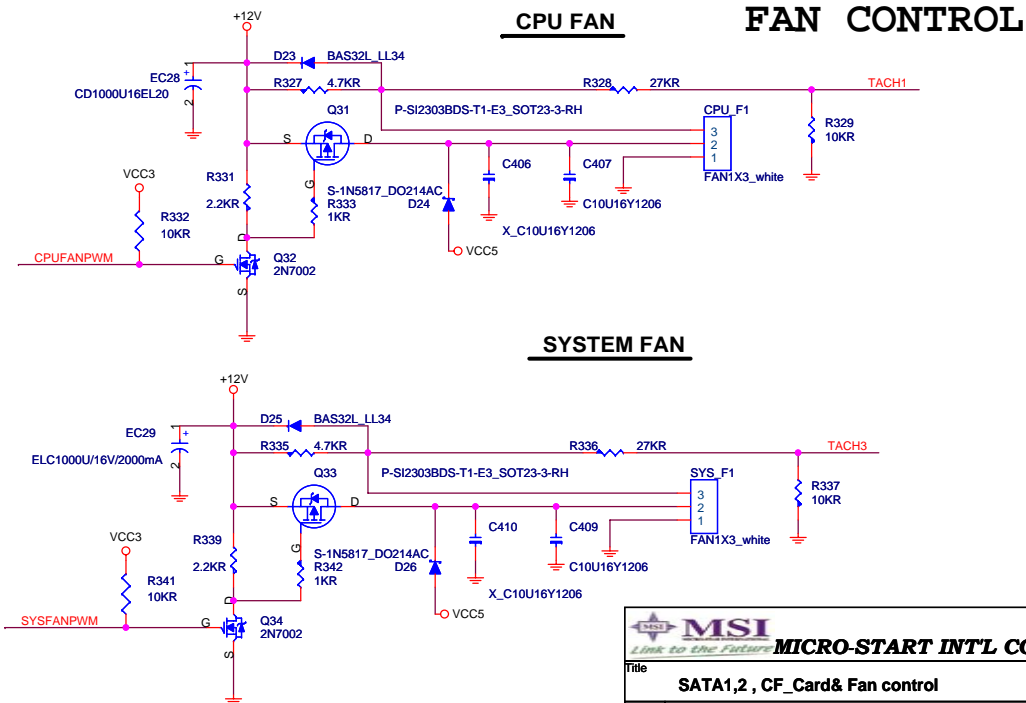
SERIAL ATA CONNECTOR BLOCK



COMPACT FLASH CONNECTOR



PLACE ADT7467 AS CLOSE AS POSSIBLE TO CPU
GUARD TRACE & D+/D- WIDTH:SPACE= 10:10 MIL(MIN)



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SATA1,2 , CF_Card& Fan control		
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ACPI Controller

DDR2 1.8V POWER...9.9A

Internal reference $V_{fb}=0.6V$ (+/- 1.5%)
Better than external reference (+/-5%)
==>Using Stand-alone mode

$$V_{fb}=V_{output}*[1.5/(1.5+3.01)]=0.6V \quad V_{output}=1.804V$$

DDR2 1.5V POWER...24.08A

$$V_{fb}=V_{output}*[2/(2+3.01)]=0.6V \quad V_{output}=1.503V$$

VTT1.1V POWER...4.9A

DDR VTT Power



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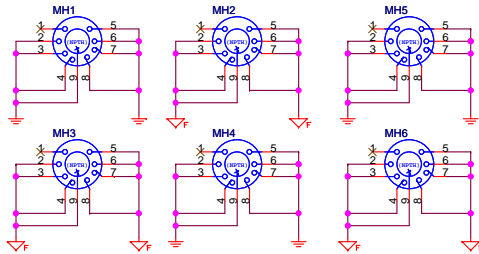
MS7 ACPI CONTROLLER

MS-7418

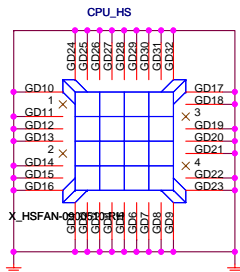
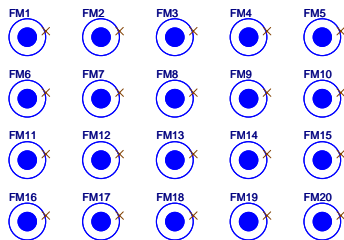
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Auto-BOM Manual Parts

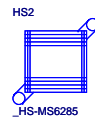
Mounting Holes



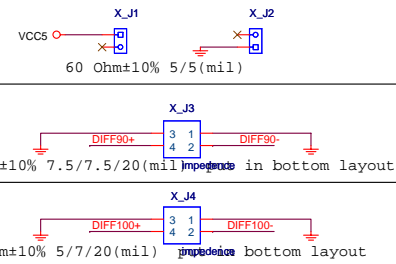
Optics Orientation Holes



NB HEAT SINK



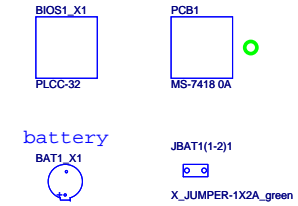
Simulation



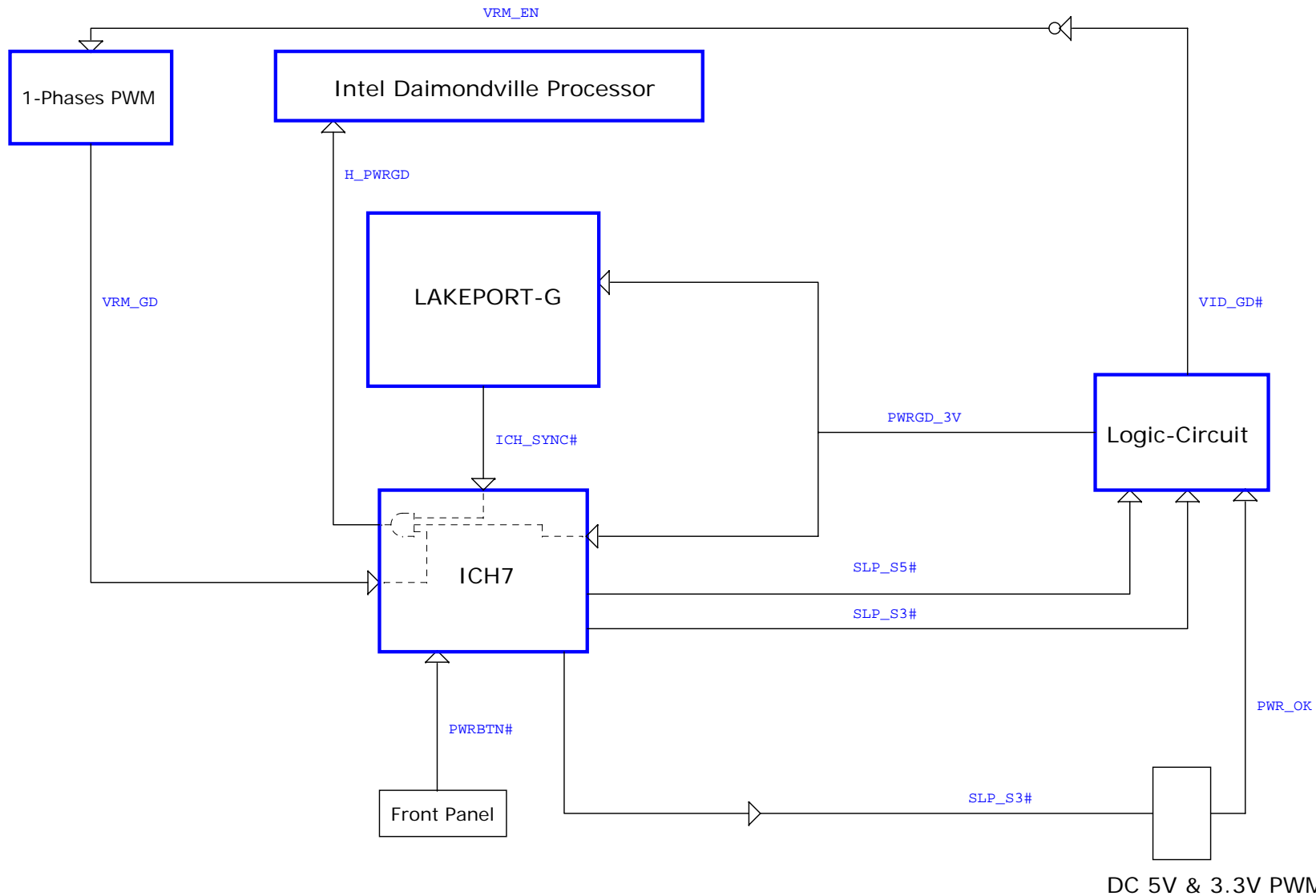
SB HEAT SINK




MANUAL PART



PWROK MAP



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